

Serial No. 09/801,639  
Amdt. dated December 14, 2004  
Reply to Office Action of September 16, 2004

Docket No. P-0195

**In the Abstract:**

*Please replace the abstract with the following amended abstract.*

An inter-processor communication apparatus of a mobile communication system including a data-FIFO configured to be directly coupled to a transmission bus and configured to store a receiving data from a master. Also included is a slave-logic configured to control a writing operation of the receiving data for the data-FIFO and count a length of the receiving data until an end-tap signal is inputted, a length-FIFO directly connected to the slave-logic and configured to store the data length counted by the slave-logic, and a CPU separately connected to the slave-logic, the data-FIFO and the length-FIFO and configured to continuously read the data stored in the data-FIFO as much as the data read from the length-FIFO when an interrupt signal is inputted from the slave-logic.